

wherein said channel semiconductor layer comprises a non-single crystalline silicon semiconductor layer containing oxygen, nitrogen or carbon at a concentration  $5 \times 10^{19}$  atoms/cm<sup>3</sup> or less and said semiconductor layer shows a Raman peak at a wavenumber of 512 cm<sup>-1</sup> or higher.

*Docket H2*  
24. The thin film transistor of claim 23 wherein said channel semiconductor layer is formed on an insulating surface of a substrate.

*Sub D2*  
*Cont D1*  
25. The thin film transistor comprising:  
a channel semiconductor layer comprising:  
a gate insulating layer contacting said channel layer; and  
a gate electrode adjacent to said channel layer with said gate insulating layer therebetween,  
wherein said channel semiconductor layer comprises a non-single crystalline silicon semiconductor layer containing oxygen, nitrogen or carbon at a concentration  $5 \times 10^{19}$  atoms/cm<sup>3</sup> or less and a ratio of a full band width at half maximum (FWHM) of a Raman peak of said channel semiconductor layer to a FWHM of a Raman peak of a single crystalline silicon is less than 3.

*Docket H4*  
26. The thin film transistor of claim 25 wherein said channel semiconductor layer is formed on an insulating surface of a substrate.

*Sub D3*  
27. A thin film transistor comprising:  
a channel semiconductor layer comprising:  
a gate insulating layer contacting said channel layer; and  
a gate electrode adjacent to said channel layer with said gate